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EXAMINER	
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ART UNIT	PAPER NUMBER
2133	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,776	SMITH, KENNETH KAY	
	Examiner	Art Unit	
	Marshall S Eng	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1.1 The drawings are objected to because both Figure 5 and Figure 6 contain the phrase "BCD Codes". This is a typo and should be changed to "BCH Codes."

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Information Disclosure Statement

2.1 The information disclosure statement filed 16 August 2001 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Specifically, reference 1Q was not included.

Claim Objections

3.1 Claim 13 is objected to because of the following informalities: the claim contains limitations within parentheses and therefore not given patentable weight.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

4.1 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4.2 Claim 1 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The data structure is not claimed as embodied in computer-readable media and is not statutory because they are not capable of causing functional change in the computer.

See MPEP 2106 Section IV-B-1(a).

4.3 Claims 4, 21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The divider is described fully in the specifications as conceptual in nature and used to be symbolic for reorganization of the logical relationship between the payload and redundancy, see lines 17-20 of page 9. The divider is essentially an abstract idea that is therefore non statutory.

Claim Rejections - 35 USC § 103

5.1 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.2 Claim(s) 1, 2 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. U.S. Patent No. 6,477,669 (hereinafter Agarwal)

As per claim 1,

Agarwal substantially teaches of a payload and of redundancy (error correction code), see lines 30-40 column 6.

Agarwal does not explicitly teach of the data being in a data structure or of a divider between the payload and the redundancy capable of being moved to produce

two different ratios of payload to redundancy data. Nonetheless, Agarwal does teach of the data frame being a fixed n bytes long, see line 30 of column 6 with a payload that has a variable length which depends on the size of the forward error correction code, see lines 33-37 of column 6.

Nonetheless, data storage and data communication use similar techniques to ensure the error free communication (read/writes) of codewords. When reading the claim without the divider, one skilled in the art sees that there exists a payload and a redundancy that can be in one of two configurations in which each configuration has a different ratio of payload to redundancy. When read in this light, it is clear that Agarwal teaches of the limitations of this claim. Specifically, in lines 33-37 of column 6, Agarwal teaches of the data frame being a fixed n bytes long, see line 30 of column 6 with a payload that has a variable length which depends on the size of the forward error correction code. By having a variable length payload that depends on the size of the fec code, it is clear that Agarwal is teaching of plural configurations in which the ratio of payload to redundancy is different.

As per claim 2,

Agarwal teaches of the redundancy containing a first error correction code (when a divider is in a first location) and containing a second error correction code (when the divider is in a second location), see lines 35-50 of column 7 where the forward error correction code is varied.

5.3 Claim(s) 3,4,5,7 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. U.S. Patent No. 6,477,669 (hereinafter Agarwal)

As per claim 3,

Agarwal substantially teaches of associating an initial error correcting code with a redundancy, see lines 25-38 of column 8. Specifically Agarwal teaches of setting the error correction code to its maximum value until synchronization is achieved. Agarwal is essentially using the worst-case scenario to set up the initial error correcting code. Agarwal further teaches of replacing (adjusted) the initial error correcting code with an updated one, see lines 35-50 of column 7 where Agarwal teaches of reducing or increasing the error correcting code length depending on channel conditions.

While Agarwal does not explicitly teach of this occurring within a data storage device, Agarwal does teach of the method occurring in data transmission. As is known in the art, data storage and data communication use similar techniques to ensure the error free communication (read/writes) of codewords.

As per claim 4,

When reading the claim without the divider, one skilled in the art sees that there exists a payload and a redundancy wherein the size of the payload and redundancy can be changed in response to the updating of the error correcting code. When interpreted this way, it is clear that Agarwal teaches the limitations of the claim. In lines 35-50 of column 7, Agarwal teaches of reducing or increasing the length of the error correction code and therefore increasing or reducing the size of the payload in response to channel conditions.

As per claim 5,

It would have been obvious to one of ordinary skill in the art at the time the invention was made to reorganize the address space shared by the payload and the redundancy to provide space required by the updated error correcting code. One of ordinary skill in the art would want to reorganize the address space so as to increase/decrease the amount of error correcting code used to protect the data payload. Obviously, one of ordinary skill would want the address space reorganized so as to be able to tell the difference between the payload and redundant data (i.e. have the beginning of the redundancy addressed correctly so as to not point at payload data and have the end of the payload data addressed correctly so as to not point at the redundancy). Only with the correct addressing of payload and redundancy can one of ordinary skill use the redundancy correctly so as to be able to correctly determine if the data has any errors.

As per claim 7,

Agarwal further teaches of tracking the errors made to determine if the initial error correction code is sufficient, see lines 35-50 of column 7, specifically where Agarwal teaches of varying the amount of error correction in accordance with the quality of the communication link. Agarwal is essentially changing the strength of the error correction code by tracking the errors and making the error correction stronger (i.e. more redundancy) if the conditions are poor (and therefore causing more errors), and making it weaker (i.e. less redundancy) if the conditions are ideal.

5.4 Claim(s) 6, 8 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. U.S. Patent No. 6,477,669 (hereinafter Agarwal) in view of admitted prior art 'Specifications' (hereinafter specs).

As per claim 6,

Agarwal substantially teaches, as above in claim 3, of associating an initial error correcting code with a redundancy, see lines 25-38 of column 8. Specifically Agarwal teaches of setting the error correction code to its maximum value until synchronization is achieved. Agarwal is essentially using the worst-case scenario to set up the initial error correcting code. Agarwal further teaches of replacing (adjusted) the initial error correcting code with an updated one, see lines 35-50 of column 7 where Agarwal teaches of reducing or increasing the error correcting code length depending on channel conditions.

Agarwal does not teach of using a memory test on data storage to determine if the initial error correction code is sufficient. Nonetheless, Agarwal does teach of adjusting the error correction code in accordance to channel conditions, see lines 35-50 of column 7.

Specs teaches of using the fundamental error rate to determine the quantity of resources devoted to the redundancy, see lines 24+ of page 1. As is known in the art, memory tests are frequently done on memory to determine the number of errors that a memory contains.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Agarwal to include the use of the

fundamental error rate (and subsequently a memory test) as taught by Specs. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Specs that the fundamental error rate of a data storage media is the rate at which errors are found within the media. With the adaptive error correcting code of Agarwal implemented within a data storage device (memory), it would have been obvious to one or ordinary skill to use a memory test to determine the conditions of the memory (similar to determining the conditions of the transmission channel). With Specs stating that the fundamental error rate is used to determine the resources devoted to redundancy, it would have obvious to one of ordinary skill to use a memory test to determine the number of errors present on a memory device.

As per claim 8,

Specs further teaches of using the media age and number or reads/writes as further examples of things that help determine the fundamental error rates, see line 27 of page 1 – line 5 of page 2. As stated above in claim 6 and in Specs, the fundamental error rate is used to help determine the amount of redundancy to use. Further, Specs teaches that for some storage devices, the fundamental error rate increases over time or after a certain number of writes and reads, see lines 8-10 of page 2.

5.5 Claim(s) 9,11 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. U.S. Patent No. 6,477,669 (hereinafter Agarwal)

As per claim 9,

Agarwal substantially teaches of a payload and of redundancy (error correction code), see lines 30-40 column 6. Agarwal further teaches of altering (varying) the amount of error correction code used, see lines 35-50 of column 7.

Agarwal does not explicitly teach of the data being in a storage device or specifically of a ratio being defined as the payload to (payload + redundancy). Nonetheless, Agarwal does teach of the data frame being a fixed n bytes long, see line 30 of column 6 with a payload that has a variable length which depends on the size of the forward error correction code, see lines 33-37 of column 6.

While Agarwal does not teach of the data being within a storage device, and instead in a transmission system, it would have been obvious to one of ordinary skill at the time the invention was made to implement the system of Agarwal in a storage device. Both data communication and data storage attempt to successfully transmit/store data by using error correcting/detecting techniques. As such, one skilled in the art would further know that the techniques used by one (i.e. data communication) are analogous to those used by the other (data storage) to help produce error free data.

Further, one skilled in the art would know that error correcting codes are often referred to as a specific rate (ratio) code, i.e. ½, 2/3, ¾, etc... where the first number is data and the second being total of (data + check). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to define the types of redundancies with a ratio of payload to (payload + redundancy). With this, for one skilled in the art to change the amount of redundancy used, it is clear that one would have to change the ratio (rate).

As per claim 11,

Agarwal further teaches of tracking the errors made to determine if the initial error correction code is sufficient, see lines 35-50 of column 7, specifically where Agarwal teaches of varying the amount of error correction in accordance with the quality of the communication link. Agarwal is essentially changing the strength of the error correction code by tracking the errors and making the error correction stronger (i.e. more redundancy) if the conditions are poor, and making it weaker (i.e. less redundancy) if the conditions are ideal.

5.6 Claim(s) 10, 12 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. U.S. Patent No. 6,477,669 (hereinafter Agarwal) in view of admitted prior art 'Specifications' (hereinafter specs).

As per claim 10,

Agarwal substantially teaches, as above in claim 9, of a payload and of redundancy (error correction code), see lines 30-40 column 6. Agarwal further teaches of altering (varying) the amount of error correction code used, see lines 35-50 of column 7.

Agarwal does not teach of using a memory test on data storage to determine if the initial error correction code is sufficient. Nonetheless, Agarwal does teach of adjusting the error correction code in accordance to channel conditions, see lines 35-50 of column 7.

Specs teaches of using the fundamental error rate to determine the quantity of resources devoted to the redundancy, see lines 24-26 of page 1. As is known in the art,

memory tests are frequently done on memory to determine the number of errors that a memory contains.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Agarwal to include the use of the fundamental error rate (and subsequently a memory test) as taught by Specs. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Specs that the fundamental error rate of a data storage media is the rate at which errors are found within the media. With the adaptive error correcting code of Agarwal implemented within a data storage device (memory), it would have been obvious to one or ordinary skill to use a memory test to determine the conditions of the memory (similar to determining the conditions of the transmission channel). With Specs stating that the fundamental error rate is used to determine the resources devoted to redundancy, it would have obvious to one of ordinary skill to use a memory test to determine the number of errors present on a memory device.

As per claim 12,

Specs further teaches of using the media age and number or reads/writes as further examples of things that help determine the fundamental error rates, see line 27 of page 1 – line 5 of page 2. As stated above in claim 10 and in Specs, the fundamental error rate is used to help determine the amount of redundancy to use. Further, Specs teaches that for some storage devices, the fundamental error rate increases over time or after a certain number of writes and reads, see lines 8-10 of page 2.

5.7 Claim(s) 13,14,18 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. U.S. Patent No. 6,477,669 (hereinafter Agarwal)

As per claim 13,

Agarwal substantially teaches of updating the initial error correcting code to replace the initial error correcting code in response to a changed error rate (i.e. change in channel condition/quality leading to more or less errors), see lines 35-50 of column 7 and lines 28-38 of column 8. Agarwal further teaches of an ECC library containing at least two ECCs that may be selected as the updated error correcting code, see lines 25-60 of column 10 where Figure 3, a table with bit error rates and the related code length are shown, is described as a table that indexes a bit error rate to a error correcting code length.

Agarwal does not explicitly teach of the method as being implemented within hardware devices such as ECC assignment modules or ECC libraries. Nonetheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method in a variety of hardware devices. As is known in the art, one skilled in the art would easily be able to implement a method in hardware once the method is found/determined.

As per claim 14,

Agarwal further teaches of using an initial error correcting code in response to an initial error rate (i.e. the assumption that to use the maximum error correcting code until sync is achieved), see lines 25-38 of column 8.

Again, Agarwal does not explicitly teach of the method as being implemented within hardware devices such as ECC assignment modules or ECC libraries. Nonetheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method in a variety of hardware devices. As is known in the art, one skilled in the art would easily be able to implement a method in hardware once the method is found/determined.

As per claim 18,

Agarwal further teaches of tracking the errors made to and reporting the error information to allow the size/strength of the code be changed, see lines 35-50 of column 7, specifically where Agarwal teaches of varying the amount of error correction in accordance with the quality of the communication link. Agarwal is essentially changing the strength of the error correction code by tracking the errors and making the error correction stronger (i.e. more redundancy) if the conditions are poor, and making it weaker (i.e. less redundancy) if the conditions are ideal.

Again, Agarwal does not explicitly teach of the method as being implemented within hardware devices such as an error tracking module. Nonetheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method in a variety of hardware devices. As is known in the art, one skilled in the art would easily be able to implement a method in hardware once the method is found/determined.

5.8 Claim(s) 15, 16, 17, 19 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. U.S. Patent No. 6,477,669 (hereinafter Agarwal) in view of admitted prior art 'Specifications' (hereinafter specs).

As per claim 15,

Agarwal substantially teaches, as taught above in claim 13, of updating the initial error correcting code to replace the initial error correcting code in response to a changed error rate (i.e. change in channel condition/quality leading to more or less errors), see lines 35-50 of column 7 and lines 28-38 of column 8. Agarwal further teaches of an ECC library containing at least two ECCs that may be selected as the updated error correcting code, see lines 25-60 of column 10 where Figure 3, a table with bit error rates and the related code length are shown, is described as a table that indexes a bit error rate to a error correcting code length. Agarwal further teaches of using an initial error correcting code in response to an initial error rate (i.e. the assumption that to use the maximum error correcting code until sync is achieved), see lines 25-38 of column 8.

Agarwal does not teach of using a technology type determination or of reporting the findings to allow an update of error correction codes. Nonetheless, Agarwal does teach of adjusting the error correction code in accordance to channel conditions, see lines 35-50 of column 7.

Specs teaches of using the fundamental error rate to determine the quantity of resources devoted to the redundancy, see lines 24-26 of page 1. Further, Specs

teaches that technology type as an example of factors that help determine the fundamental error rate, see line 27 of page 1 – line 1 of page 2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Agarwal to include the use of the fundamental error rate as taught by Specs. Further, Specs teaches of the various factors that can influence the fundamental error rate, see line 27 of page 1 – line 5 of page 2. This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Specs that technology type (as well as other factors see line 27 of page 1 – line 5 of page 2) are used to help determine the fundamental error rate. With the adaptive error correcting code of Agarwal implemented within a data storage device (memory), it would have been obvious to one of ordinary skill to use any and all of the dependant factors to determine the fundamental error rate. By using these factors, one skilled in the art would be able to make an accurate estimation of the fundamental error rate, enabling him/her to be able to allocate an appropriate amount of redundancy.

Further once the method of Agarwal is implemented within hardware, it would have been obvious to send the results to a device that can interpret the results and make appropriate adjustments to the error correcting code, if necessary.

As per claim 16,

Specs further teaches of using the fundamental error rate to determine the quantity of resources devoted to the redundancy, see lines 24-26 of page 1. As is known in the art, memory tests are frequently done on memory to determine the number

of errors that a memory contains. Clearly, since the fundamental error rate is the rate at which errors occur, it would have been obvious to one skilled in the art to use memory tests to help determine the number (and rate) of errors on the storage device. After completing a memory test, one skilled in the art would be able to make a more accurate estimation of the fundamental error rate, enabling him/her to be able to allocate an appropriate amount of redundancy.

Again, Agarwal does not explicitly teach of the method as being implemented within hardware devices such as a memory test module. Nonetheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method in a variety of hardware devices. As is known in the art, one skilled in the art would easily be able to implement a method in hardware once the method is found/determined.

As per claim 17,

Specs further teaches of using the application type (technology type, which the Examiner is interpreting as expected technology, and hence use, that the memory will have) as a further example of things that help determine the fundamental error rates, see line 27 of page 1 – line 5 of page 2. As stated above in claim 16 and in Specs, the fundamental error rate is used to help determine the amount of redundancy to use, see lines 24-26 of page 1.

Further once the method of Agarwal is implemented within hardware, it would have been obvious to send the information about application determination to an updater to make appropriate adjustments to the error correcting code.

As per claim 19,

Specs further teaches of using the media age and number or reads/writes as further examples of things that help determine the fundamental error rates, see line 27 of page 1 – line 5 of page 2. As stated above in claim 16 and in Specs, the fundamental error rate is used to help determine the amount of redundancy to use, see lines 24-26 of page 1. Further, Specs teaches that for some storage devices, the fundamental error rate increases over time or after a certain number of writes and reads, see lines 8-10 of page 2.

Further once the method of Agarwal is implemented within hardware, it would have been obvious to send the information about age and use to an updater to make appropriate adjustments to the error correcting code.

5.9 Claim(s) 20 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. U.S. Patent No. 6,477,669 (hereinafter Agarwal) in view of admitted prior art 'Specifications' (hereinafter specs).

As per claim 20,

Agarwal substantially teaches of an ECC library containing at least two ECCs that may be selected as the updated error correcting code, see lines 25-60 of column 10 where Figure 3, a table with bit error rates and the related code length are shown, is described as a table that indexes a bit error rate to a error correcting code length. Agarwal further teaches of using an initial error correcting code in response to an initial error rate (i.e. the assumption that to use the maximum error correcting code until sync is achieved), see lines 25-38 of column 8. Agarwal substantially teaches of updating

the initial error correcting code to replace the initial error correcting code in response to a changed error rate (i.e. change in channel condition/quality leading to more or less errors), see lines 35-50 of column 7 and lines 28-38 of column 8. Agarwal further teaches of tracking the errors made to and reporting the error information to allow the size/strength of the code be changed, see lines 35-50 of column 7, specifically where Agarwal teaches of varying the amount of error correction in accordance with the quality of the communication link. Agarwal is essentially changing the strength of the error correction code by tracking the errors and making the error correction stronger (i.e. more redundancy) if the conditions are poor, and making it weaker (i.e. less redundancy) if the conditions are ideal.

Agarwal does not explicitly teach of using technology type determination, application type determination, a memory test, age and use tracking, or updated application tracking to help determine if an updated error correcting code is needed.

Specs teaches of using the fundamental error rate to determine the quantity of resources devoted to the redundancy, see lines 24-26 of page 1. Further, Specs teaches that technology type as an example of factors that help determine the fundamental error rate, see line 27 of page 1 – line 5 of page 2. Specs further teaches of using the application type (technology type, which the Examiner is interpreting as expected technology, and hence use, that the memory will have) as a further example of things that help determine the fundamental error rates, see line 27 of page 1 – line 5 of page 2. As stated above in claim 16 and in Specs, the fundamental error rate is used to help determine the amount of redundancy to use. Specs further teaches of using the

fundamental error rate to determine the quantity of resources devoted to the redundancy, see lines 24-26 of page 1. As is known in the art, memory tests are frequently done on memory to determine the number of errors that a memory contains. Clearly, since the fundamental error rate is the rate at which errors occur, it would have been obvious to one skilled in the art to use memory tests to help determine the number (and rate) of errors on the storage device. After completing a memory test, one skilled in the art would be able to make a more accurate estimation of the fundamental error rate, enabling him/her to be able to allocate an appropriate amount of redundancy. Specs further teaches of using the media age and number or reads/writes as further examples of things that help determine the fundamental error rates, see line 27 of page 1 – line 5 of page 2. As stated above in claim 16 and in Specs, the fundamental error rate is used to help determine the amount of redundancy to use. Further, Specs teaches that for some storage devices, the fundamental error rate increases over time or after a certain number of writes and reads, see lines 8-10 of page 2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Agarwal to include the use of the fundamental error rate as taught by Specs. Specifically, Specs teaches of the various factors that can influence the fundamental error rate (technology type, media age, number of writes/reads, etc...). This modification would have been obvious because one of ordinary skill in the art would have been motivated by the suggestion provided by Specs that technology type (as well as other factors see line 27 of page 1 – line 5 of page 2) are used to help determine the fundamental error rate. With the adaptive error

correcting code of Agarwal implemented within a data storage device (memory), it would have been obvious to one of ordinary skill to use any and all of the dependant factors to determine the fundamental error rate. By using these factors, one skilled in the art would be able to make an accurate estimation of the fundamental error rate, enabling him/her to be able to allocate an appropriate amount of redundancy.

Further, it would have been obvious to one skilled in the art to continue tracking the application of the media to determine if the error correction code being used is sufficient. By initially selecting a level of error correction based on the expected application, it is obvious that the application can have an impact on the amount of error correction needed. Therefore, one skilled in the art would be motivated to continue monitoring the application so as to be able change the level of error correction being used. One skilled in the art would see this as being comparable to monitoring the condition of a channel, as taught by Agarwal, and changing the level of error correction depending on the state of the channel.

Further once the method of Agarwal is implemented within hardware, it would have been obvious to send the results to a device that can interpret the results and make appropriate adjustments to the error correcting code, if necessary.

5.10 Claim(s) 21-22 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Agarwal et al. U.S. Patent No. 6,477,669 (hereinafter Agarwal)

As per claim 21,

Agarwal substantially teaches of associating an initial error correcting code with a redundancy, see lines 25-38 of column 8. Specifically Agarwal teaches of setting the

error correction code to its maximum value until synchronization is achieved. Agarwal is essentially using the worst-case scenario to set up the initial error correcting code. Agarwal further teaches of updating the initial error correcting code to replace the initial error correcting code in response to a changed error rate (i.e. change in channel condition/quality leading to more or less errors), see lines 35-50 of column 7 and lines 28-38 of column 8.

When reading the claim without the divider, one skilled in the art sees that there exists a payload and a redundancy wherein the size of the payload and redundancy can be changed in response to the updating of the error correcting code. When interpreted this way, it is clear that Agarwal teaches the limitations of the claim. In lines 35-50 of column 7, Agarwal teaches of reducing or increasing the length of the error correction code and therefore increasing or reducing the size of the payload in response to channel conditions.

Agarwal does not explicitly teach of the method as being implemented within/on a computer-readable medium capable of being executed. Nonetheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method on a computer-readable medium capable of being executed. As is known in the art, one skilled in the art would easily be able to implement a method in/on a computer-readable medium once the method is found/determined.

As per claim 22,

Agarwal teaches of monitoring (tracking) the errors (and error rate, see lines 45-55 of column 8) made to determine if the initial error correction code is sufficient, see

lines 35-50 of column 7, specifically where Agarwal teaches of varying the amount of error correction in accordance with the quality of the communication link. Agarwal is essentially changing the strength of the error correction code by tracking the errors and making the error correction stronger (i.e. more redundancy) if the conditions are poor, and making it weaker (i.e. less redundancy) if the conditions are ideal. Agarwal further teaches of altering (varying) the amount of error correction code used, see lines 35-50 of column 7. Agarwal further teaches of providing a level of redundancy (i.e. error correcting cod size/length) appropriate to the measured error rate, see lines 5-10 of column 10.

Agarwal does not explicitly teach of the method as being implemented within/on a computer-readable medium capable of being executed. Nonetheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the method on a computer-readable medium capable of being executed. As is known in the art, one skilled in the art would easily be able to implement a method in/on a computer-readable medium once the method is found/determined.

Conclusion

6.1 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Fukasawa et al. U.S. Patent No. 4,701,923

This reference teaches of selecting error correcting codes in response to frame error rate detected during communication.

b. Hassner et al. U.S. Patent No. 6,651,213

This reference teaches of adaptively controlling the level of error correction redundancy.

c. Ayanoglu et al. U.S. Patent No. 5,600,663

This reference teaches of adaptively changing the number of parity bits, bytes or packets based upon prior error patterns.

d. Klayman et al. U.S. Patent No. 5,699,365

This reference teaches of adaptive forward error correction where a revised fec is selected when a channel parameter is met.

e. Stewart U.S. Patent No. 5,912,907

This reference teaches of changing the error correcting code rate if proper decoding does not occur at the current rate.

f. "Error Doing – 4 Properties and performance of polynomial codes" document.

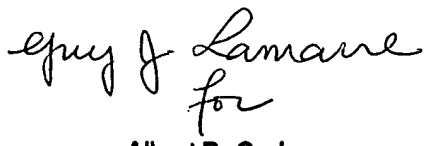
This reference teaches of modified codes, specifically of expurgated codes on page 4. Expurgated codes, as is known in the art, are codes in which data bits are replaced by parity bits where the initial size of the packet/codeword remains constant.

6.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marshall S Eng whose telephone number is (703) 305-4638. The examiner can normally be reached on M-Th, 8:30 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

mse



Albert DeCady
Primary Examiner